Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A method for managing an external memory of a microprocessor to achieve more available capacity, the method comprising:

(a) providing an address translator;

(b) using the address translator to translate a page of the external memory and an address within the page pointed by the microprocessor to a physical address of the external memory, each common area pointed by the microprocessor being mapped to a section of the external memory; and

(c) using the microprocessor to access data stored at the physical address of the external memory.

[c2] 2.The method of claim 1 wherein the section of the external memory is common area of the external memory, and the external memory has only one common area.

[c3] 3.The method of claim 2 wherein the external memory has a plurality of non-common areas.

4.The method of claim 2 further comprising mapping the page of the external memory and the address of the common area of the page pointed by the microprocessor

of the microprocessor to the physical address of the common area of the external memory.

[c4] 5.The method of claim 1 wherein the microprocessor processes an instruction set of 8 bits.

[c5] 6.The method of claim 1 wherein the microprocessor is an MCS series microprocessor.

[c6] 7.The method of claim 1 wherein the external memory is a flash memory.

[c7] 8. A chip for executing the method of claim 1.